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Our ref.: 0503-A30213us/final/spin(王琮郁)/Nelson

**METHOD OF FORMING GATE OXIDE LAYERS WITH MULTIPLE THICKNESSES**

**ON SUBSTRATE**

**BACKGROUND**

The present invention relates to a semiconductor process,  
5 and particularly to a method of forming gate oxide layers with  
multiple thicknesses on a substrate.

In order to increase the performance of integrated circuits  
(ICs), circuit designers often require gate devices with various  
characteristics. Such various characteristics can be achieved  
10 with different gate dielectric layer thicknesses, such that the  
gate devices can be operated at differing voltage levels.  
Conventionally, high voltage devices are formed on a wafer with  
a relatively thick gate dielectric layer to prevent breakdown  
during the high voltage operation. On the other hand, low  
15 voltage devices are formed on the same wafer with a relatively  
thin gate dielectric layer to increase the speed of the circuit.

FIGS. 1a to 1d are cross-sections showing a conventional  
method of forming integrated circuit gate dielectric layers with  
multiple thicknesses. In FIG. 1a, a substrate 100, such as a

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silicon wafer, is provided. A plurality of shallow trench isolation (STI) structures 102 composed of oxides is formed within the substrate 100. As a result, active regions 10 and 20 are defined on the substrate 100 and separated from each other by the isolation structure 102. Here, the active region 10 is used as a device region for high voltage operation, such as a power device region. Moreover, the active region 20 is used as a device region for low voltage operation, such as an input/output (I/O) or core device region.

10 In FIG. 1b, conventional thermal oxidation is performed on the substrate 100 to form a relatively thick oxide layer 104 on the active regions 10 and 20. The formed oxide layer 104 is used as a gate dielectric layer for the subsequent high voltage device fabrication. Next, a photoresist layer 106 is formed overlying  
15 the oxide layer 104 and the STI structures 102, which has an opening 107 over the active region 20 to expose the overlying oxide layer 104. However, a high voltage (for example, 40V) device commonly requires a gate dielectric layer with a thickness more than 1000Å to prevent breakdown during high  
20 voltage operation. The gate dielectric layer formed by

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conventional thermal oxidation may greatly increase the thermal budget, thus increasing the fabricating cost. Moreover, the thick thermal oxide layer 104 causes the corners 102a of the STI structures 102 to round off, negatively impacting device properties and narrowing the areas of the active regions 10 and 20.

Next, in FIG. 1c, the exposed oxide layer 104 on the active region 20 is removed by, for example, wet chemical etching using the hydrofluoric acid (HF) as an etchant. During the wet etching, the STI structures 102 composed oxides are also etched, resulting in the loss of a portion of the STI structures 102, depicted as the recess regions 102b in FIG. 1c. The recess regions 102b may expose a portion of the active region 20 at the corners, inducing leakage current and decreasing device reliability.

Finally, in FIG. 1d, after the photoresist layer 106 is stripped by conventional process, thermal oxidation is performed on the exposed substrate 100 on the active region 20 to form a relatively thin oxide layer 108 thereon. Thereafter, the poly gates 110 and 112 are respectively formed on the gate

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dielectric layers corresponding to the active region 10 and the active region 20 by conventional processes to complete the high and low voltage gate devices fabrication.

U.S. Pat. No. 5, 672, 561 to Barsan et al. discloses a method  
5 of forming gate oxide layers with multiple thicknesses on a wafer substrate, which employs multiple doping regions with various impurities to prompt or retard the thermal oxidation on each doping region. As mentioned above, however, this approach still uses thermal oxidation to form the gate oxide layer. Since the  
10 thickness of the gate oxide layer for high voltage devices is greater than 1000Å, the thermal budget is greatly increased. Moreover, it is difficult to form suitable gate oxide thicknesses for the low voltage devices while simultaneously forming the gate oxide layers for the high and low voltage  
15 devices, even when using nitrogen ion implantation to retard oxide formation on the low voltage device region.

Additionally, U.S. Pat. No. 6,541,321 to Buller et al. discloses a method for forming multiple gate oxide layers with the plasma oxygen doping, while U.S. Pat. No. 6,593,182 to Chen  
20 discloses a method of making transistors with gate insulation

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layers of differing thickness. Such methods use oxygen or  
fluorine atoms to prompt the thermal oxidation, thereby forming  
gate dielectric layers with different thicknesses. Also,  
however, the thermal budget and other problems as mentioned  
5 above still cannot be effectively solved.

It is therefore apparent that the art is in need of an  
improved process capable of solving problems, so as to increase  
reliability of ICs having gate devices with different operation  
voltage levels.

10

#### SUMMARY

Accordingly, one object of the present invention is to form  
gate devices with multiple thickness dielectric layers on a  
substrate for different operation voltage levels.

Another object of the present invention is to form gate  
15 dielectric layers with various thickness on a substrate using  
a composite oxide as the gate dielectric layer for the high  
voltage device, thereby reducing thermal budget and preventing  
the formation of recesses in shallow trench isolation (STI)  
regions.

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The above and other objects and advantages, which will be apparent to one of skill in the art, are achieved in the present invention which is directed to, in a first aspect, a method of forming dielectric layers with various thicknesses on a substrate. First, a first device region and a second device region are provided on the substrate. Next, a first oxide layer is grown on the substrate. A dielectric layer with a first thickness is subsequently deposited on the first oxide layer. Thereafter, the dielectric layer and the underlying first oxide layer on the second device region are removed to expose the substrate. Finally, a second oxide layer with a second thickness less than the first thickness is formed on the substrate of the second device region.

In another aspect of the invention, a method of forming gate dielectric layers with various thicknesses on a substrate is provided. First, a first active region and a second active region are provided on the substrate. Next, a first thermal oxide layer is formed on the substrate. A blanket dielectric layer with a first thickness is deposited overlying the substrate. Next, a first masking layer is formed overlying the

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substrate except over the second active region. The dielectric layer and the underlying first thermal oxide layer on the second active region are successively etched using the first masking layer as an etch mask to expose the substrate. The first masking  
5 layer is subsequently removed. Thereafter, a second thermal oxide layer with a second thickness less than the first thickness is formed on the second active region. Finally, a first gate is formed on the dielectric layer on the first active region and a second gate is formed on the second thermal oxide layer on the  
10 second active region.

In yet another aspect of the invention, a method of forming an integrated circuit having gate oxide layers with multiple thicknesses is provided. First, a substrate having a first active region, a second active region, and a third active region  
15 is provided. A first oxidation is performed to form a first oxide layer on the substrate and a blanket high temperature oxide layer with a first thickness is then deposited overlying the substrate. Next, a first photoresist layer is formed on the high temperature oxide layer except over the second active region.  
20 The high temperature oxide layer and the underlying first oxide

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layer on the second active region are successively etched using  
the first photoresist layer as an etch mask to expose the  
substrate, and the first photoresist layer is then removed.  
Next, a second oxidation is performed to form a second oxide  
5 layer with a second thickness less than the first thickness on  
the second active region. Next, a second photoresist layer is  
formed overlying the substrate except over the third active  
region. Thereafter, the high temperature oxide layer and the  
underlying first oxide layer on the third active region are  
10 successively etched to expose the substrate, and the second  
photoresist layer is then removed. Next, a third oxidation is  
performed to form a third oxide layer with a third thickness less  
than the first thickness on the third active region and on the  
second oxide layer on the second active region. Finally, a first  
15 gate is formed on the high temperature oxide layer on the first  
active region, a second gate is formed on the second oxide layer  
on the second active region, and a third gate is formed on the  
third thermal oxide layer on the third active region.



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### BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, given by way of illustration only and thus not intended to be limitative of the present invention.

FIGS. 1a to 1d are cross-sections showing a conventional method of forming an integrated circuit having gate dielectric layers with multiple thicknesses.

FIGS. 2a to 2e are cross-sections showing a method of forming an integrated circuit having gate dielectric layers with multiple thicknesses according to the invention.

### DESCRIPTION

In FIG. 2a, a substrate 200, such as a silicon substrate or other semiconductor substrate, is provided. An isolation region composed of a plurality of isolation structures 202 is formed within the substrate 200 by conventional isolation technology.

For example, the isolation structures 202 can be a field oxide (FOX) formed by shallow trenches isolation (STI) or local

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oxidation of silicon (LOCOS), wherein STI is preferable. As a result, a plurality of active regions is defined on the substrate 200 and separated from each other by the isolation structures 202. Here, in order to simplify the diagram, three active regions 30, 40, and 50 and three isolation structures 202 are depicted in FIG. 2a. In the invention, the active region 30 is used as a device region for high voltage (for example, 40V) operation, such as a power device region. Moreover, the active region 40 is used as a device region for low voltage (for example, 5.0V) operation, such as an input/output (I/O) device region. Furthermore, the active region 50 is used as a device region for even lower voltage (for example, 2.5V) operation, such as a core device region. Additionally, prior to the step depicted in FIG. 2a, various ion implantations and annealing processes may be performed to form desired well regions within the substrate 200 for MOS device fabrication.

Next, in FIG. 2b, a thin oxide layer 204 is formed on the active regions 30, 40, and 50. Here, the thin oxide layer 204 can be formed by performing a thermal oxidation on the substrate 200 and has a thickness of about 40 to 60Å. In the invention,

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the thin oxide layer 204 on the active region 30 is used as a portion of the gate dielectric layer for the subsequent high voltage device (for example, power device) fabrication.

Thereafter, a critical step of the invention is performed.

5 A blanket dielectric layer 206 is formed on the isolation structures 202 and the oxide layer 204. In the invention, the dielectric layer 206 can be a thick oxide layer formed by conventional physical or chemical deposition technology. For example, the dielectric layer 206 is a high temperature oxide  
10 (HTO) layer formed by chemical vapor deposition using tetraethyl orthosilicate (TEOS) as a deposition precursor at a temperature of about 700 to 900°C. The dielectric layer 206 on the active region 30 is used as the major portion of the gate dielectric layer for the subsequent high voltage device fabrication. That  
15 is, in the invention, the gate dielectric layer of the high voltage device is a composite oxide layer comprising a thermal oxide layer 204 and an overlying high temperature oxide layer 206. The thickness of the dielectric layer 206 depends on the design rule for the high voltage device fabrication. In general,  
20 the dielectric layer 206 has a thickness of about 300 to 1200Å

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if the operation voltage is about 20 to 40V. Since the major portion of the gate dielectric layer is formed by CVD rather than by thermal oxidation in the prior art, the thermal budget may be greatly reduced.

5           Next, in FIG. 2c, a masking layer 208, such as a photoresist layer, is formed on the blanket dielectric layer 206 by conventional lithography. The masking layer 208 has an opening to expose the underlying dielectric layer 206 on the active region 40. Thereafter, the exposed dielectric layer 206 and the  
10           underlying oxide layer 204 on the active region 40 is removed by conventional dry or wet chemical etching using the masking layer 208 as an etch mask to expose the substrate 200 on the active region 40. In the invention, for example, the exposed dielectric layer 206 and the underlying thin oxide layer 204 is  
15           removed by wet chemical etching using hydrofluoric acid (HF) or buffer oxide etching (BOE) solution as an etchant. Since the dielectric layer 206 is also deposited on the isolation structures 202 adjacent to the active region 40, the isolation structures 202 composed of oxides can be protected from the  
20           formation of recesses during the wet chemical etching.

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Next, in FIG. 2d, the photoresist layer 208, which is no longer needed, is removed by conventional ashing or suitable solution. A thin oxide layer 210 is subsequently formed on the exposed substrate 200 on the active region 40. Here, the thin  
5 oxide layer 210 can be formed by performing a thermal oxidation on the substrate 200 and has a thickness of about 40 to 70Å. In the invention, the thin oxide layer 210 on the active region 40 is used as a portion of the gate dielectric layer for the subsequent low voltage device (for example, I/O device)  
10 fabrication.

A blanket masking layer 212, such as a photoresist layer, is subsequently formed overlying the substrate 200. Next, the masking layer 212 is patterned by conventional lithography to expose the dielectric layer 206 on the active region 50.  
15 Thereafter, the exposed dielectric layer 206 and the underlying oxide layer 204 on the active region 50 is removed by conventional dry or wet chemical wet etching using the masking layer 212 as an etch mask to expose the substrate 200 on the active region 50. In the invention, the exposed dielectric layer  
20 206 and the underlying oxide layer 204 can be removed by wet

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chemical etching using HF or BOE solution as an etchant. Also,  
since the dielectric layer 206 is also deposited on the isolation  
structures 202 adjacent to the active region 50, the isolation  
structures 202 composed of oxides can be protected from the  
5 formation of recesses during the wet chemical etching.

Finally, in FIG. 2e, a thin oxide layer 214 is subsequently  
formed on the exposed substrate 200 on the active region 50 and  
on the oxide layer 210 on the active region 40. Here, the thin  
oxide layer 214 can be formed by performing a thermal oxidation  
10 on the substrate 200 and the oxide layer 210, and has a thickness  
of about 40 to 60Å if the operation voltage is about 2.5V. In  
the invention, the thin oxide layer 214 on the active region 50  
is used as the gate dielectric layer for the subsequent low  
voltage device (for example, core device) fabrication.  
15 Moreover, the thin oxide layer 214 on the active region 40 is  
used as another portion of the gate dielectric layer for the  
subsequent I/O device fabrication. That is, the gate dielectric  
layer of the I/O device is composed of the oxide layer 214 and  
the underlying oxide layer 210, which has a thickness of about  
20 80 to 130Å if the operation voltage is about 5V. Next, poly gates

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216, 218, and 220 are respectively formed on the gate dielectric layers corresponding to the high voltage device region 30 and the low voltage regions 40 and 50 by conventional processes. As a result, the integrated circuit gate dielectric layers with multiple thicknesses is completed.

According to the invention, the gate dielectric layer of the high voltage device is a composite oxide and the major portion of the gate dielectric layer is formed by CVD rather than by thermal oxidation in the prior art. Accordingly, the thermal budget is greatly reduced to reducing the fabricating cost.

Moreover, in the invention, the relatively thin thermal oxide layer is formed on the active regions firstly, rather than a relatively thick thermal oxide layer in the prior art, preventing rounding off of the corners of the STI structures and narrowing of the active regions.

Furthermore, the blanket dielectric layer formed by CVD can serve as a sacrificial layer to protect the underlying STI structures when exposing the substrate on the active regions by etching, thereby preventing recessing of the STI structures. Accordingly, reliability of the devices can be increased.

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While the invention has been described by way of example  
and in terms of the preferred embodiments, it is to be understood  
that the invention is not limited to the disclosed embodiments.  
To the contrary, it is intended to cover various modifications  
5 and similar arrangements (as would be apparent to those skilled  
in the art). Therefore, the scope of the appended claims should  
be accorded the broadest interpretation so as to encompass all  
such modifications and similar arrangements.